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Design and Implementation of Bridge PFC Boost Converter

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Abstract: *A systematic review of bridge power factor correction (PFC) boost rectifiers is presented in this paper. Both open-loop and closed-loop controlled boost converters are modeled and simulated using the Simulink blocks. The bridge PFC topologies may reduce the conduction loss by reducing the number of semiconductor components. The bridge PFC boost implementations have received increased attention. In each circuit, the boost converter is implemented by replacing a pair of bridge rectifiers with switches and employing an AC side boost inductor. The construction and implementation of these PFC boost rectifiers are fairly easy, which can prove useful in the real world.*

Keywords: *power factor correction (PFC) boost rectifiers, continuous conduction mode (CCM)*

I. Introduction

Recently, in an effort to improve the efficiency of front-end PFC rectifiers, several power supply manufacturers and some semiconductor companies have started looking into bridge PFC circuit topologies. As the number of equipment using conventional diode rectifiers increases, harmonic input currents are becoming problematic. In an effort to meet these requirements, power-factor correction techniques to reduce harmonic current are becoming increasingly important. Furthermore, it is desirable to have minimal size, high efficiency, and a low electromagnetic interface. A few topologies have been introduced to meet these requirements. A bridge input power factor boost converter has been introduced over the potential for higher efficiency to meet the increasing demands of power savings, especially in switch-mode power supply applications.

Generally, bridge PFC topologies reduce conduction loss by reducing the number of semiconductor components. The bridge PFC boost implementations have received increasing attention recently. In each circuit, the boost converter is implemented by replacing a pair of bridge rectifiers with switches and by employing an AC side boost inductor. The bridge circuit is analyzed, designed, and simulated with resistive load. The circuit has certain advantages such as reduced conduction loss, reduced harmonics, and improved power factor. Experimental results based on prototype are obtained to show the performance of the controller. In this study, a systematic review of bridge PFC boost rectifier implementations that have received the most attention is presented. Power factor correctors are widely used as the first stage in several AC-DC power supply systems. With these converters, the injection of current harmonics to the line is very low.

If the specification requires a fast output voltage regulation, a second stage is needed to improve the output converter dynamics. The DC-DC converter placed in cascade defines the two-stage converter output voltage response. There are numerous applications in which the load remains more or less constant and hence an extremely fast output voltage response is not needed. In some of these applications, a PFC can be used for designing a low-cost, complete power supply in the 100 W ranges. However, this option has some limitations. Hence, a PFC can be used as a single circuit to perform a complete power supply if:

i) The PFC has a galvanic isolation (i.e., based on a DC-DC converter with a transformer, namely the Fly-back family of converters).
ii) The output voltage is sufficiently high or the output ripple specification is not very restrictive.
iii) The dynamic requirements can be achieved by a PFC.

II. Bridge Boost Converter Open-Loop And Closed-Loop Diagrams

Figure 1 shows the boost converter simulation circuit where the output voltage is greater than the input voltage. A boost converter is also called a step-up converter. A large inductor in series with the source voltage is essential. When the switch is on, the input current flows through the inductor and the switch, and the inductor stores the energy during this period. When the switch is off, the inductor current cannot die down instantaneously; hence, this current is forced to flow through the diode and the load during this off period. As the current tends to decrease, polarity of the emf is induced in Lb is reversed. As a result, voltage across the load is the sum of supply voltage and inductor voltage, and it is greater than the supply voltage. The voltage impressed across the inductor during the on-period is Vd.

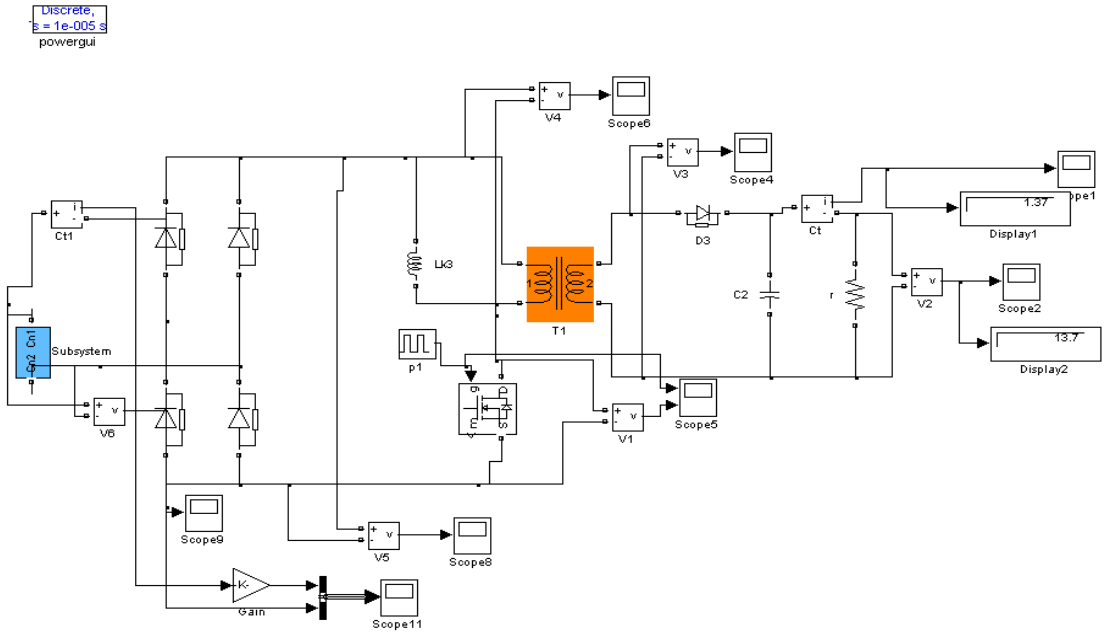

Figure 1. Boost Converter

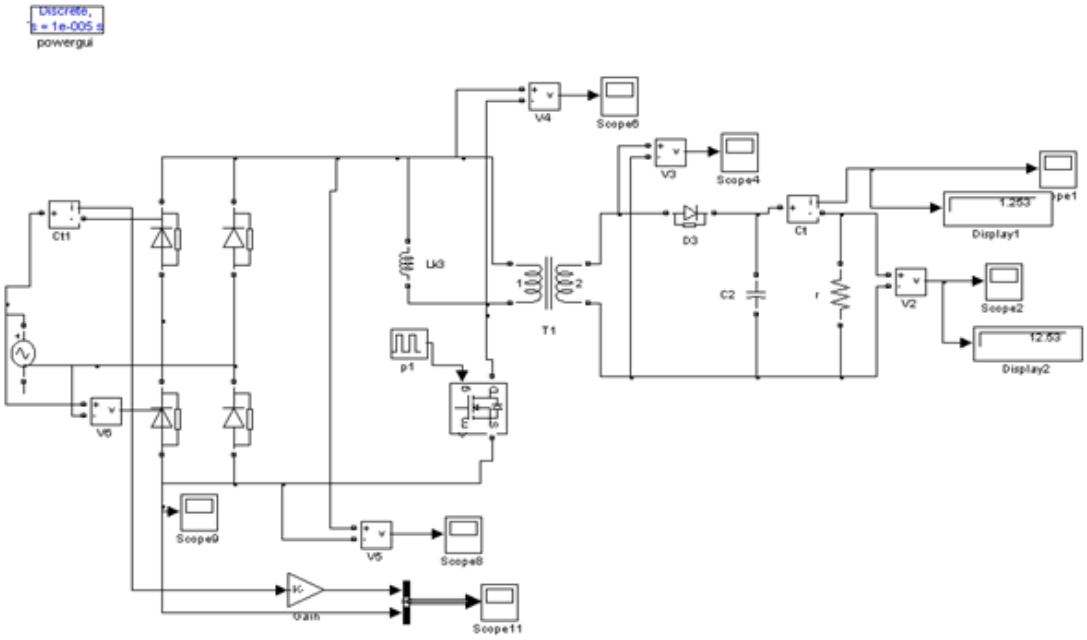

Figure2. Circuit Diagram for Open Loop

The circuit of an open-loop system is shown in Figure 2 and the circuit of a closed-loop system is shown in Figure 3. The output across the load is sensed. It is compared with the reference voltage. The error is applied to a PI controller. The output of a PI controller is given to a comparator. In the comparator, the triangular waveform is compared with the error signal to generate the pulses. The pulse width is reduced to bring the voltage to the normal value.

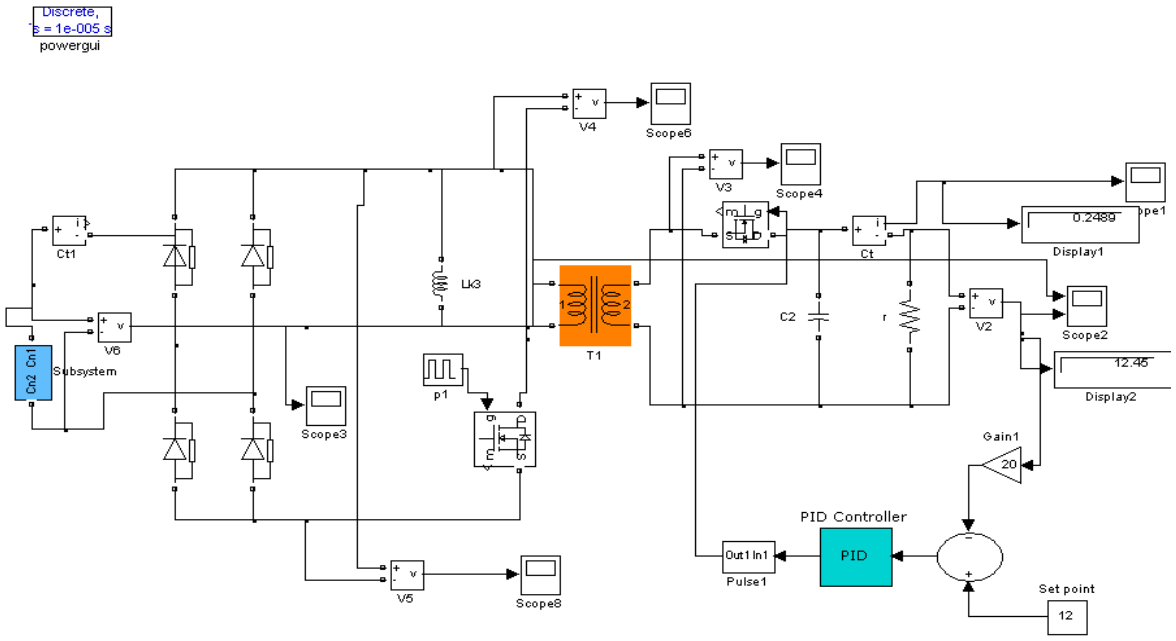

Fig.3. Circuit Diagram for Closed Loop

III. Simulation Results

The simulation circuit of a boost converter is shown in Figure 1. The AC input voltage and current wave are shown in Figure 4. The input current is in line with the AC input voltage. DC output current is shown in Figure 5. The DC output voltage is shown in Figure 6.

The simulation circuit of an open-loop system with disturbance at the input is shown in Figure 2. A step change in input voltage is applied as shown in Figure 7. The output voltage is also increased due to the changes in the input as shown in Figure 8.

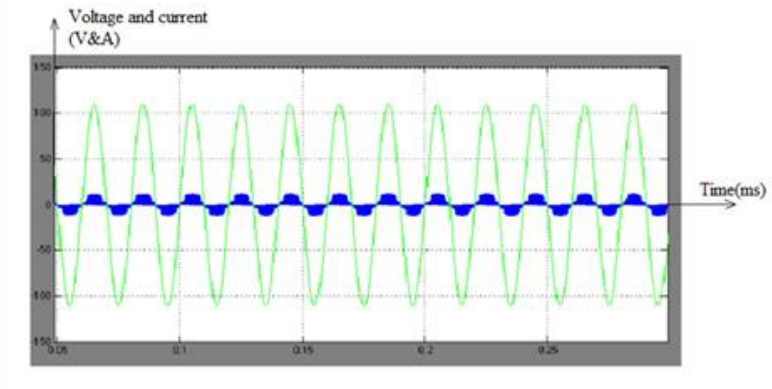

Figure 4. AC Input Voltage and Current

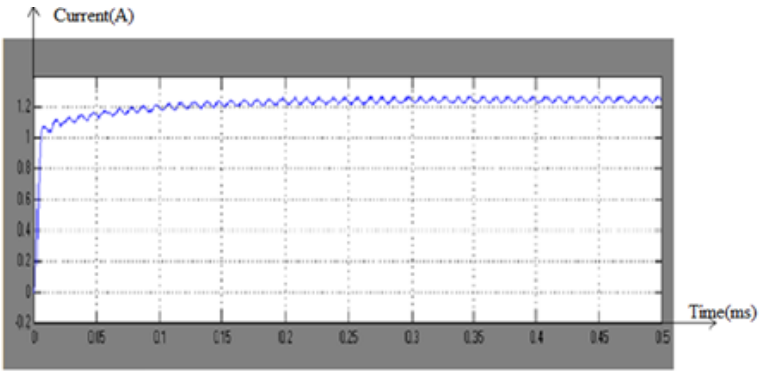

Figure 5. Output Current

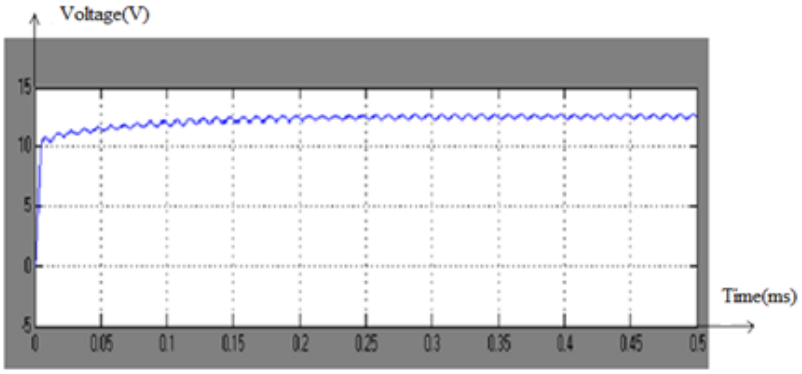

Figure 6. Output DC Voltage

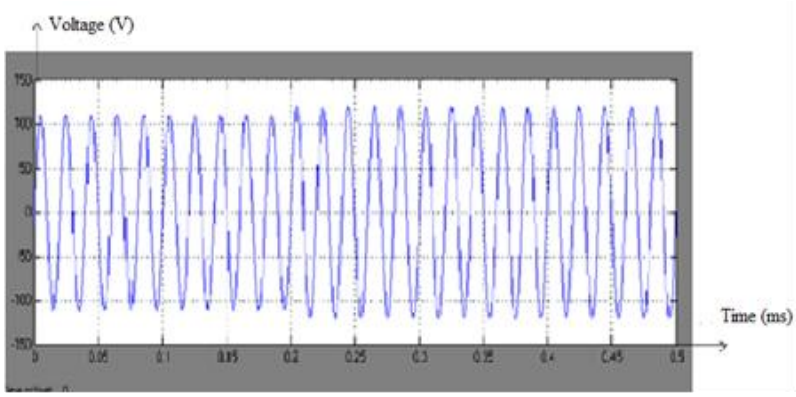

Figure 7. Input Voltage for Open Loop

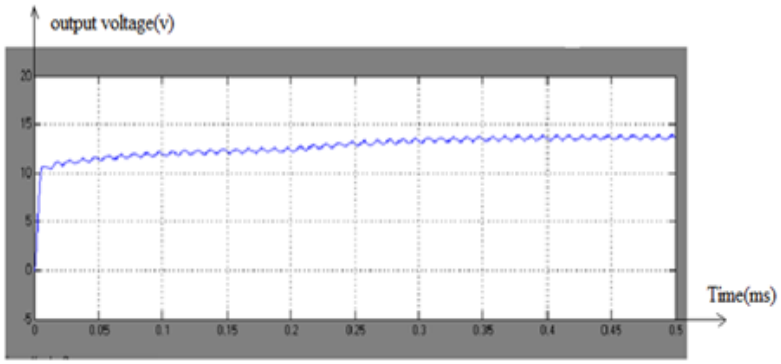

Figure 8. Output Voltage for Open Loop

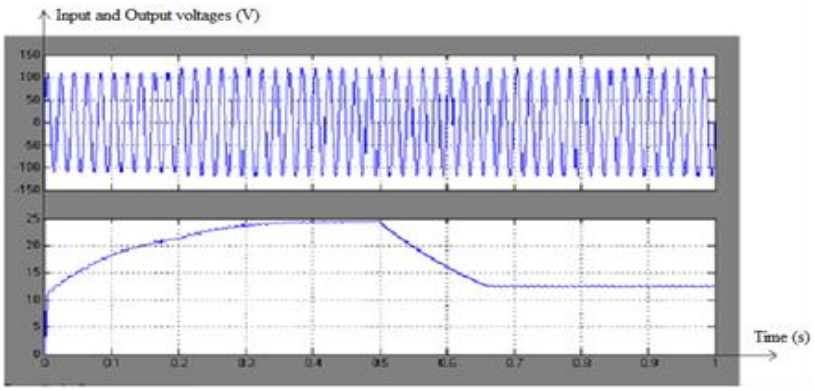

Figure 9. Input and Output Voltage for Closed Loop

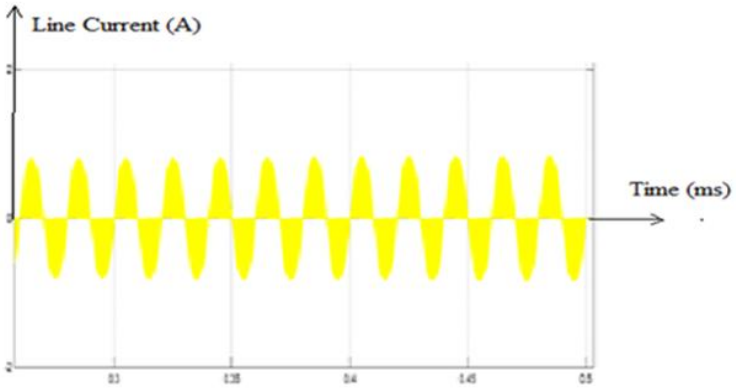

Figure 10. Line Current at 50 Hz

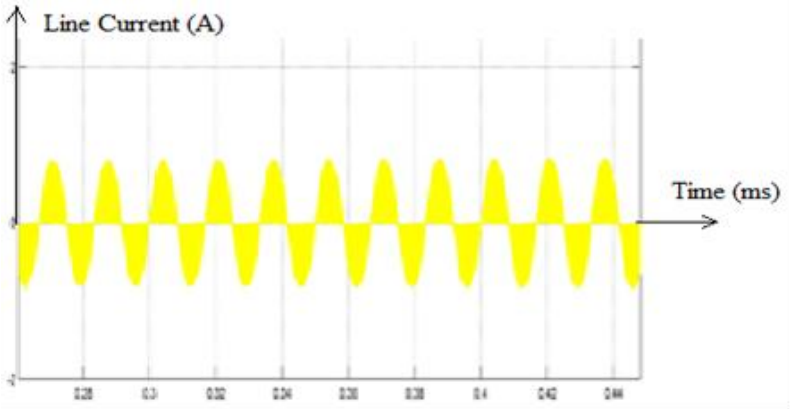

Figure 11. Line Current at 60 Hz

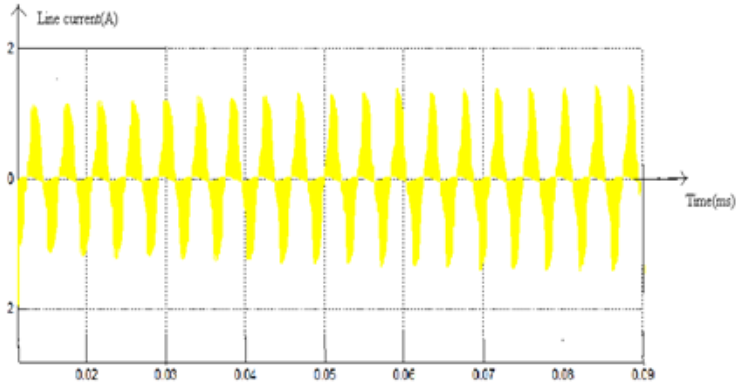

Figure 12. Line Current at 240 Hz

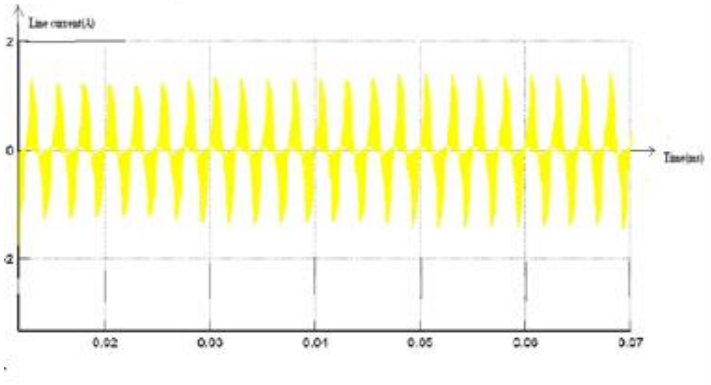

Figure 13. Line Current at 400 Hz

The simulation circuit of a closed-loop system is shown in Figure 3. The input and output voltages of the closed-loop system are shown in Figure 9. The line current at different frequencies are also shown in Figures 10–13.

IV. Hardware Implementation Of Bridge Pfc Converter

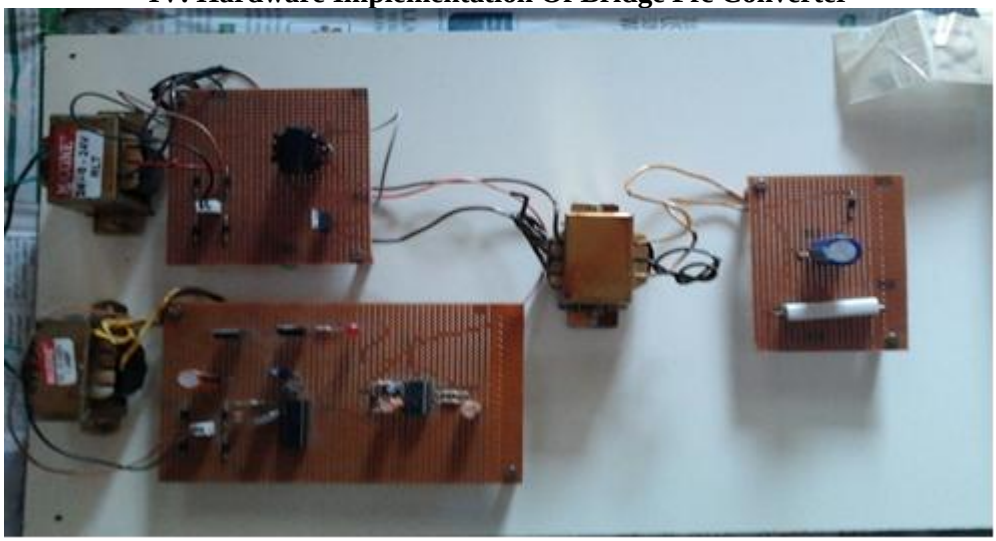

Figure14. Implemented Hardware Diagram

This section describes the hardware implementation of the proposed system. The hardware includes the Power Supply Isolation circuit and the Micro Controller Driver circuit.

The power supply is given by the step-down transformer (230/15) V whose output is rectified into the DC power and supplied to the control circuit with a voltage of +13.6 V (rms). The 15 V AC input is rectified into 15 V pulsating DC with the help of a full-bridge rectifier circuit. The ripples in the pulsating DC are removed and pure DC is obtained by using a capacitor filter. The positive terminal of the capacitor is connected to the input pin of the 7812 regulator for voltage regulation. An output voltage of 12 V obtained from the output pin of 7812 is fed as the supply to the pulse amplifier. An output voltage of 5 V obtained from the output pin of 7805 is fed as the supply to the micro controller. From the same output pin of 7805, an LED is connected in series with the resistor to indicate that the power is on.

An isolation circuit has been introduced in the circuit to avoid the interference of one signal with another and to reduce the effect of harmonics, primarily due to ripples. The configuration includes IR2110/IR2113, which are high-voltage, high-speed power MOSFET and IGBT drivers, with independent high and low side referenced output channels. Proprietary HVIC and latch-immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high-frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 500 or 600 V.

The AT89C2051 is the micro controller used in the circuit. It is a low-voltage, high-performance CMOS 8-bitmicrocomputer with 2K Bytes of Flash programmable and erasable read only memory. The device is manufactured using ATMEL high-density nonvolatile memory technology and is compatible with the industry standard MCS-51 instruction set. By combining a versatile 8-bit CPU with flash on a monolithic chip, the ATMEL AT89C2051 becomes a powerful microcomputer, which provides a highly flexible and cost-effective solution to several embedded control applications.

V. Conclusion

In this study, open-loop and closed-loop controlled boost converters are modeled and simulated using Simulink blocks; moreover, an analysis of dominant bridge PFC converter is carried out. The bridge boost rectifier has the advantage of reduced harmonics. Higher efficiency can be achieved by using the bridge boost topology. The laboratory model is implemented and the experimental results are obtained. These experimental results are correlated with the simulation results. The model with an input of 110 V (AC) is implemented. This leads to an output of 12 V (DC).The line current at different frequencies is also determined.

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